General Description

With human-machine interfacing requiring ever higher functionality and intuitiveness, touch panel type interfaces are rapidly becoming the norm for the new millennium.

TC334 is a 4 channel capacitive sensing device. The device can operate as a controller for 4 keys.

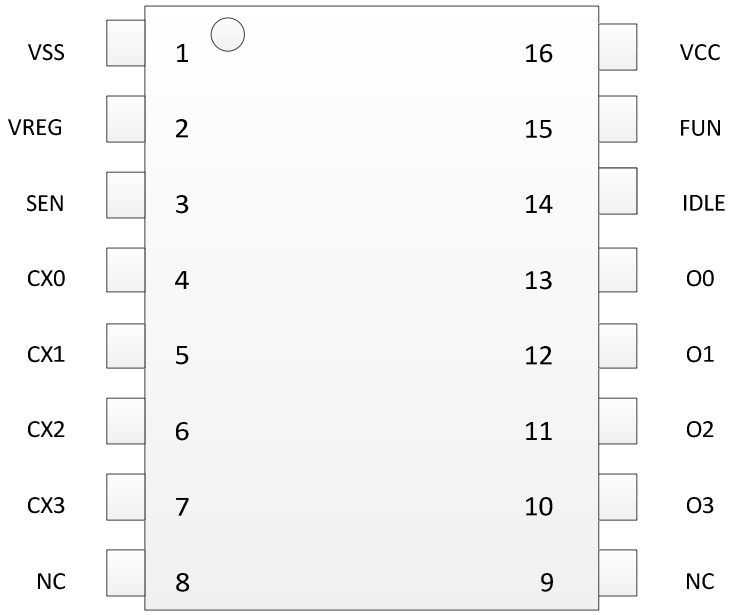
Features

- ☐ The device controls 4 completely independent touch sensing keys
- ☐ Autocal for life - no adjustments required
- ☐ System cost reduction
- ☐ Parallel outputs
- ☐ Reliability through reducing system complexity
- ☐ Embedded noise immunity circuit
- ☐ Low current consumption in IDLE state
- ☐ RoHS compliant SO-16 package

Applications

- ☐ Media Players
- ☐ Consumer Electronics
- ☐ Home appliances
- ☐ Keypads
- ☐ Mechanical switch replacement
- ☐ Sealed control panels, keypads

Pin Diagram



Pin Description

Pin	Name	I/O	Description
1	VSS	Ground	Supply Ground
2	VREG	Analog Output	Reference output
3	SEN	Analog I/O	Sensitivity Set
4	CX0	Analog I/O	sensor pad for chanel0
5	CX1	Analog I/O	sensor pad for chanel1
6	CX2	Analog I/O	sensor pad for chanel2
7	CX3	Analog I/O	sensor pad for chanel3
10	O3	Digital Output	Output for CX3(open-drain)
11	O2	Digital Output	Output for CX2(open-drain)
12	O1	Digital Output	Output for CX1(open-drain)
13	O0	Digital Output	Output for CX0(open-drain)
14	IDLE	Digital Input	IDLE state enable
15	FUN	Digital Input	Function select
16	VCC	Pwr	Power in

SEN

Sensitivity set pin , the capacitance range is 15pf ~100pf. The smaller the value the higher the sensitivity

VREG

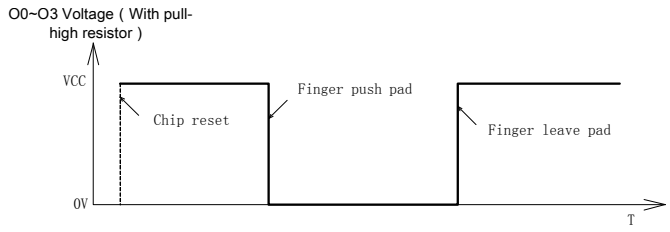
Reference voltage output, connected to 4.7nf capacitance.

CX0~CX3

Capacitive sense pins connected to electrodes. Series resistance is 3KΩ.

O0~O3

Parallel output ports of CX0~CX3 respectively. The structure of these parallel output ports is open drain NMOS for active low output level operation.



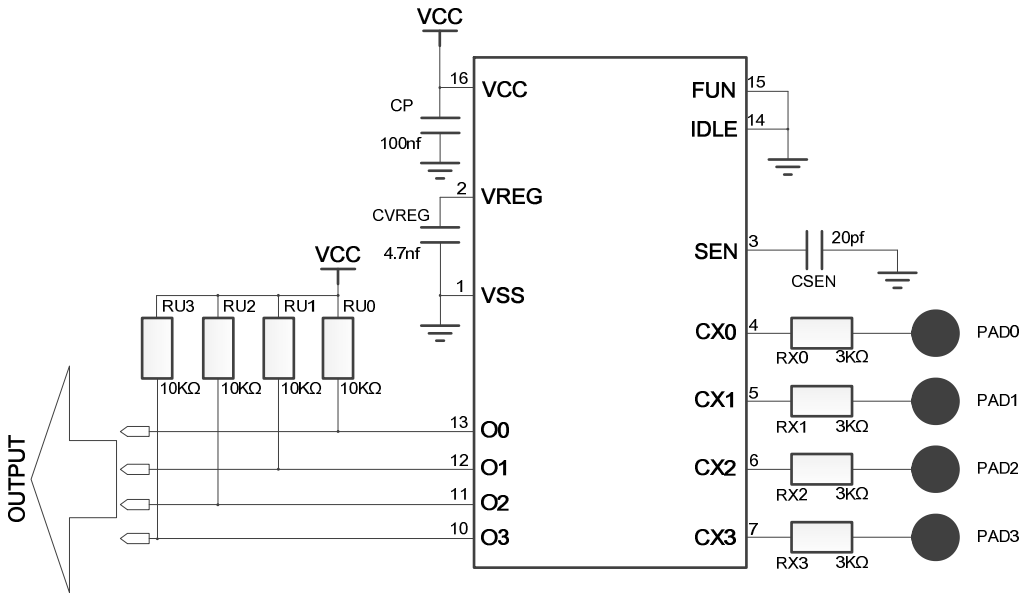
IDLE

IDLE is the enable pin of the IDLE state. If it is connected to ground, IDLE state is unable. If it is connected to VCC and no key is touched for 75S, the chip will enter IDLE state. In IDLE state the interval of sample cycle becomes larger, and the current consumption(Idd) becomes small.

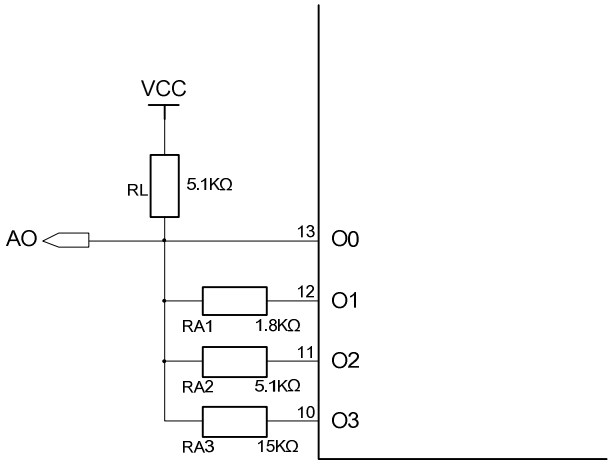
FUN

Connected to VSS

Application Circuit



Analog Voltage Output



KEY	O0	O1	O2	O3	Voltage of AO
KEY0(CX0) Pushed	LOW	High-z	High-z	High-z	0v
KEY1(CX1) Pushed	High-z	LOW	High-z	High-z	0.26*VCC
KEY2(CX2) Pushed	High-z	High-z	LOW	High-z	0.50*VCC
KEY3(CX3) Pushed	High-z	High-z	High-z	LOW	0.75*VCC
NO KEY	High-z	High-z	High-z	High-z	VCC

PCB Layout Notice

1． VCC and VSS power line should be drawn alone, and can not share power line with other chips(micro-controller and LCD driver,etc.). So as to prevent the chip from being affected by noise signal going throng the power line.

2． CP，CVREG，CSEN these three capacitances should be placed as close as possible to the chip. And the series resistors on wire of sense pad should also be placed as close as possible to the chip.

3. The larger area of grounded copper, the more immunity to noise Interference.

4. The sense traces and pad should be paid more attention to. The chip should be placed as close as possible to sense pad. The sense traces should be drawn to sense pad directly. The length of the different sense traces is not necessarily equal. The width of sense traces should be as small as possible. There should not be other power line and signal traces around the sense trace. If it can not be avoided, the other traces should cross the sense trace vertically. The distance between sense pads should be greater than 5mm. The distance between sense pad and grounded copper should be greater than 1.5mm.

Absolute Maximum Rating *

Operating temperature	-40 ~ +85ºC
Storage temp	-50 ~ +150ºC
VCC	-0.3 ~ +6.5V
Max continuous pin current, any control or drive pin	±10mA
Voltage forced onto any pin	-0.3V ~ (Vcc+ 0.3) Volts

* NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

Electrical Characteristics

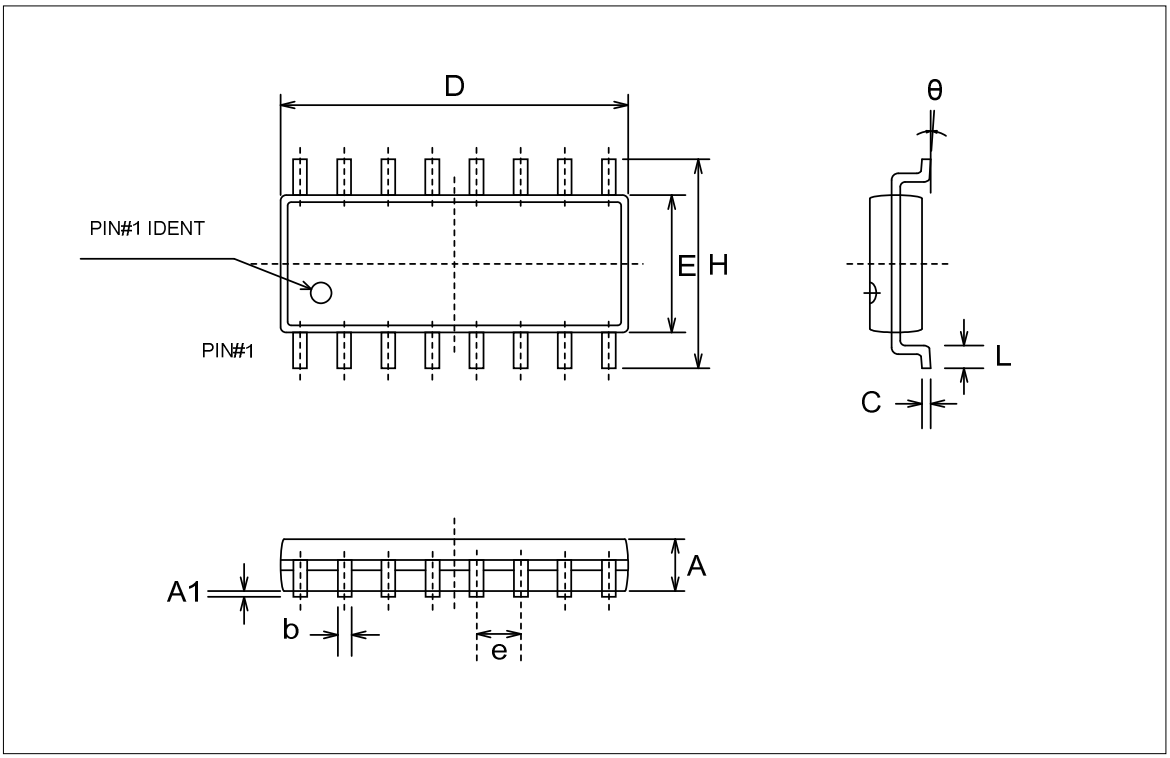
TA = 25℃

Characteristics	Symbo	Condition	Min	Typ	Max	Units
Operating voltage	Vcc		2.5		6.5	V
Current consumption	Idd	VCC=5.0V		1.0		mA
		VCC=3.0V		550		UA
		VCC=5.0V &IDLE		20		UA
		VCC=3.0V &IDLE		11		UA
Self calibration time after chip reset	Tini			120		ms
Range of capacitance on Pad	CX				2.5*CSEN	
Output impedance (open drain)	Zo	Low voltage		50		Ohm
		Hi-z		100M		
Output sink current	Isk	VCC=5V			10.0	mA
Minimum detective capacitance difference	delta_CX	CSEN=15pf		0.2		pF
Sample cycle	Tsi	Normal working state		4.5		ms
	Tsis	IDLE state		230		ms
Time of enter IDLE state	Tidle			75		s

ESD Characteristics

Mode	Polarity	Max	Reference
H.B.M	POS/NEG	8000V	VDD
		8000V	VSS
		8000V	P to P
M.M	POS/NEG	500V	VDD
		500V	VSS
		500V	P to P

Package Diagram (SO-16)



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.30	1.50	1.70	0.051	0.059	0.067
A1	0.06	0.16	0.26	0.002	0.006	0.010
b	0.30	0.40	0.55	0.012	0.016	0.022
C	0.15	0.25	0.35	0.006	0.010	0.014
D	9.70	10.00	10.30	0.382	0.394	0.406
E	3.75	3.95	4.15	.0148	0.156	0.163
e	--	1.27	--	--	0.050	--
H	5.70	6.00	6.30	0.224	0.236	0.248
L	0.45	0.65	0.85	0.018	0.026	0.033
θ	0°	--	8°	0°	--	8°