General Description

With human-machine interfacing requiring ever higher functionality and intuitiveness, touch panel type interfaces are rapidly becoming the norm for the new millennium.

TC305 is a 5 channel capacitive sensing device. The device can operate as a controller for 5 keys.

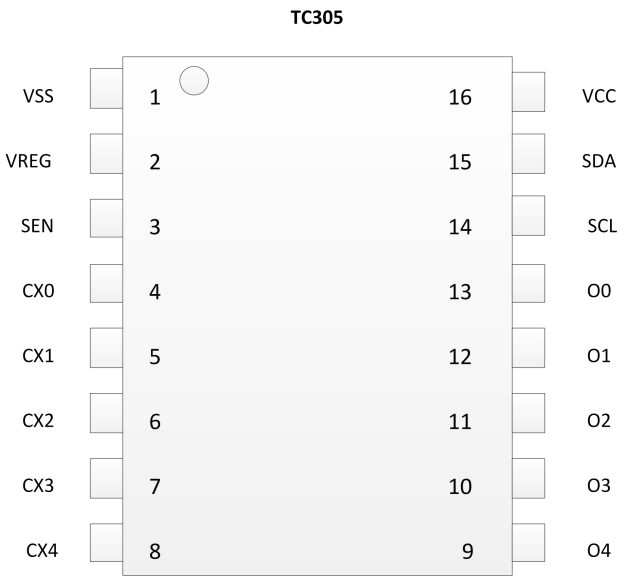
Features

- ☐ The device controls 5 completely independent touch sensing keys
- ☐ Autocal for life - no adjustments required
- ☐ System cost reduction
- ☐ I2C interface and parallel output
- ☐ Reliability through reducing system complexity
- ☐ Embedded noise immunity circuit
- ☐ Low current consumption in IDLE state
- ☐ RoHS compliant SO-16 package

Applications

- ☐ Media Players
- ☐ Consumer Electronics
- ☐ Home appliances
- ☐ Keypads
- ☐ Mechanical switch replacement
- ☐ Sealed control panels, keypads

Pin Diagram



Pin Description

Pin	Name	I/O	Description
1	VSS	Ground	Supply Ground
2	VREG	Analog Output	Reference output
3	SEN	Analog I/O	Sensitivity Set
4	CX0	Analog I/O	Sensor pad for chanel0
5	CX1	Analog I/O	Sensor pad for chanel1
6	CX2	Analog I/O	Sensor pad for chanel2
7	CX3	Analog I/O	Sensor pad for chanel3
8	CX4	Analog I/O	Sensor pad for chanel4
9	O4	Digital Output	Output for chanel4
10	O3	Digital Output	Output for chanel3
11	O2	Digital Output	Output for chanel2
12	O1	Digital Output	Output for chanel1
13	O0	Digital Output	Output for chanel0
14	SCL	Digital In	I2C clock pin
15	SDA	Digital I/O	I2C data pin
16	VCC	Pwr	Power in

SEN

Sensitivity set pin, the capacitance range is 10pf ~100pf , the smaller the value the higher the sensitivity.

VREG

Reference voltage output, connected to 4.7nf capacitance.

CX0~CX4

Capacitive sense pins connected to electrodes. Series resistance is 3KΩ.

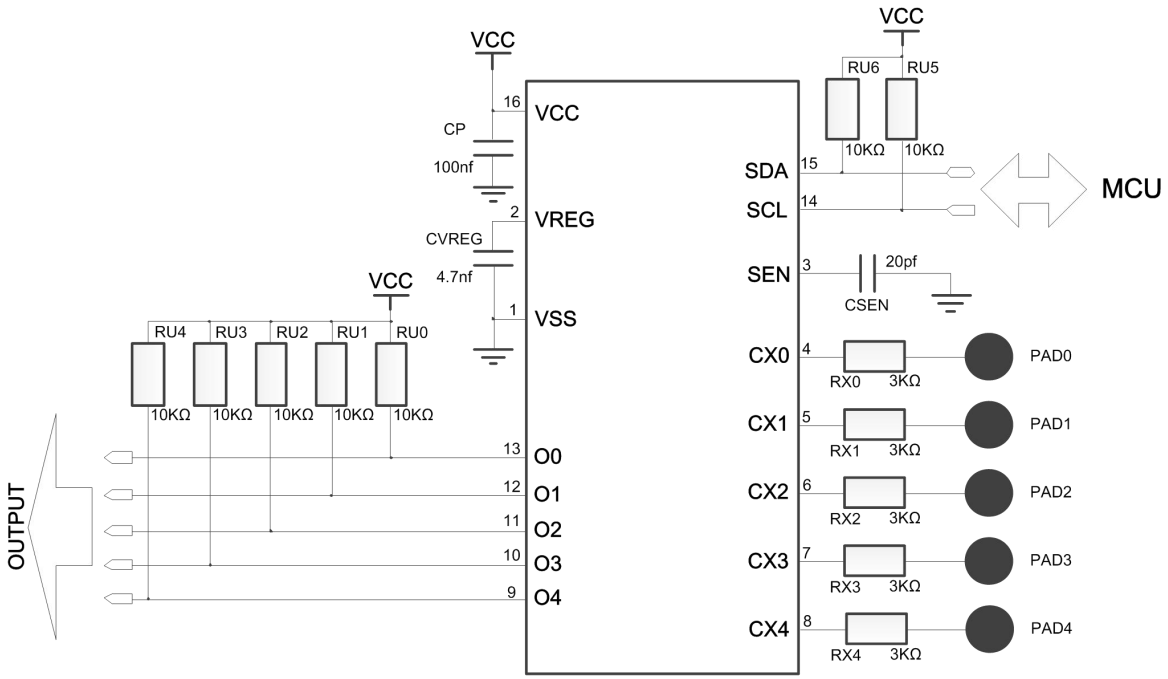
O0~O4

Parallel output ports of CX0~CX4 respectively. The structure of these parallel output ports is open drain NMOS for active low output level operation.

SCL,SDA

SCL is I2C clock input pin and SDA is I2C data I/O pin. SDA pin have a weak internal pull-up resistor.

Application Circuit



I2C Interface

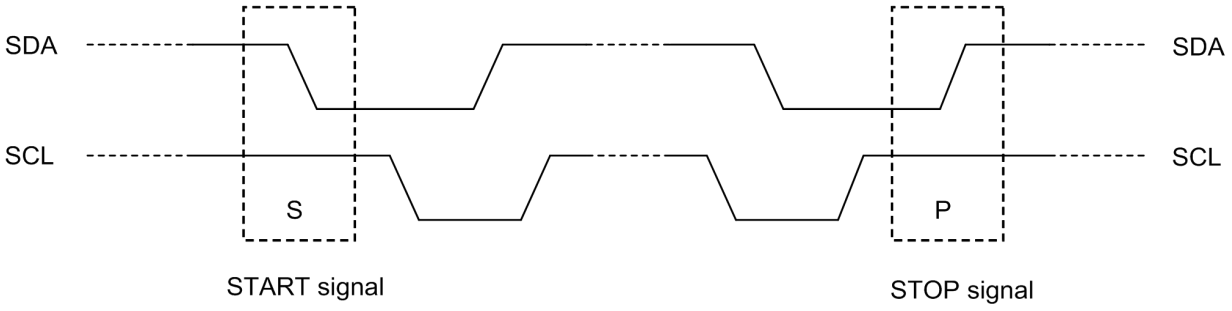
1. **Start and Stop signal**

Start signal(S)

A high to low transition on the SDA line while SCL is high defines a START condition.

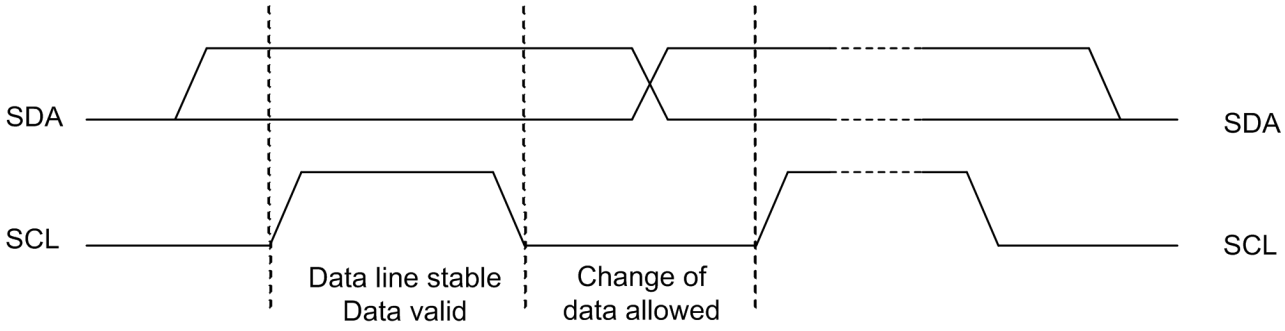
Stop signal(P)

A low to high transition on the SDA line while SCL is high defines a STOP condition.



2. Data Validity

The data on the SDA line must be stable during the high period of the SCL line. The high or low state of the SDA line can be changed when the clock signal on the SCL line is LOW.



3. Byte format

The byte structure is composed with 8 Bit data and an acknowledge signal.

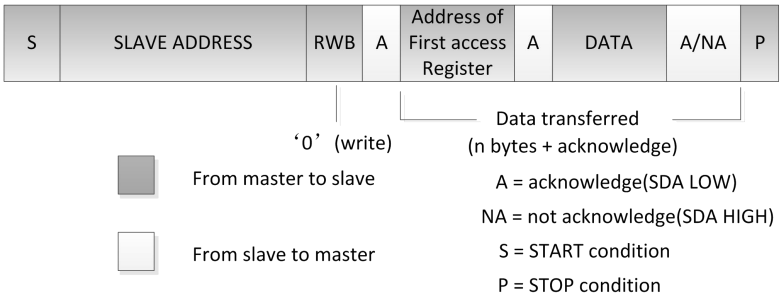
4. **Device address**

Address (A[6:0])	41H
Read command (A[6:0]+RWB)	83H
Write command (A[6:0]+RWB)	82H

5. **TC305 is a slave device, supporting Read and Write operation mode**

1) Write operation

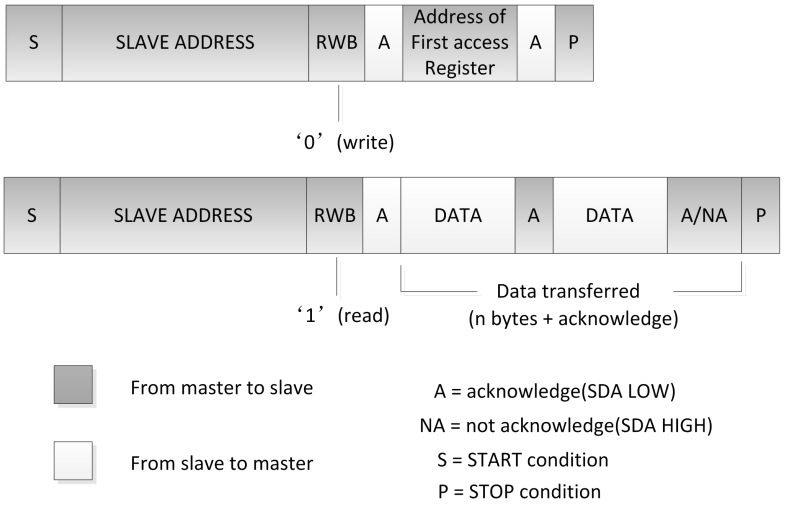
- The first byte gives the device address plus the direction bit (RWB = 0).
- The second byte contains the internal address of the first register to be accessed.
- The third byte is what to be written in the internal register.
- The transfer lasts until stop conditions are encountered.
- The TC305 acknowledges every byte transfer.



2) Read operation

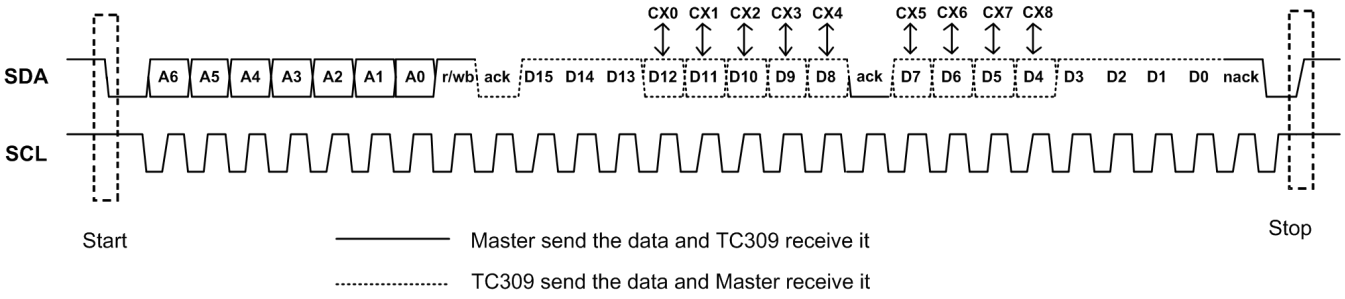
The address of the first register to read is programmed in a write operation without data, and

terminated by the stop condition. Then, another start is followed by the device address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial address.。



3) Simplified read operation

The default address of read register is 08H. So, if no other registers have been accessed, the key information can be read as the following diagram directly.



6. TC305 control registers list

Register	Address (HEX)	R/W	Initial Value(BIN)	Register function description							
				Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SenSet0	00H	W	0111 1001	SENSET0[7:0]							
SenSetCOM	01H	W	0111 1001	SENSETCOM[7:0]							
CTRL0	02H	W	100 0 0 0 11	SLPCYC[2:0]			SLPNOW	HOLD	KVF	RTM[1]	RTM[0]
Output1	08H	R	0000 0000				CH0	CH1	CH2	CH3	CH4

6.1 Sensitivity Set register SenSet0(Address 00H) SenSetCOM (Address 01H)

SENSET0[7:0] Sensitivity setting for channel CX0

SENSETCOM[7:0] Sensitivity setting for other channels

There are 16 values for setting sensitivity. Sensitivity from low to high : 04H , 15H , 25H , 36H , 47H 58H , 68H , 79H , 8AH , 9BH , ACH , BCH , CDH , DEH , EFH , FFH .The initial default value is 79H

Channel CX0 can be used as a proximity sensor because SENSET0[7:0] is independent .If channel CX0 is used as a common key, SENSET0[7:0] should be just set same as SENSETCOM[7:0]

6.2 Control register CTRL0(Address 02H)

SLPCYC[2:0] Setting for interval of sampling in idle state

SLPCYC[2:0]	0	1	2	3	4(default)	5	6	7
Sampling interval	infinite	0.5T	1.5T	2.5T	3.5T	4.5T	5.5T	6.5T

T≈120ms

SLPNOW

SLPNOW	1	0(default)
	Enter idle state right now, when no key detected	If no key is detected for 75S,then enter idle state

HOLD

HOLD	1	0(default)
	Stop auto calculation	Auto calculation for reference

6.3 Output register for key Output0 (Address 08H)

CH[4:0] Respectively corresponding to channel CX[4:0]. When key is detected ,it's zero, otherwise, it's 1.

PCB Layout Notice

1. VCC and VSS power line should be drawn alone, and can not share power line with other chips(micro-controller and LCD driver,etc.). So as to prevent the chip from being affected by noise signal going throng the power line.
2. CP，CVREG，CSEN these three capacitances should be placed as close as possible to the chip. And the series resistors on wire of sense pad should also be placed as close as possible to the chip.
3. The larger area of grounded copper, the more immunity to noise Interference.
4. The sense traces and pad should be paid more attention to. The chip should be placed as close as possible to sense pad. The sense traces should be drawn to sense pad directly. The length of the different sense traces is not necessarily equal. The width of sense traces should be as small as possible. There should not be other power line and signal traces around the sense trace. If it can not be avoided, the other traces should cross the sense trace vertically. The distance between sense pads should be greater than 5mm. The distance between sense pad and grounded copper should be greater than 1.5mm.

Absolute Maximum Rating *

Operating temperature	-40 ~ +85ºC
Storage temp	-50 ~ +150ºC
VCC	-0.3 ~ +6.5V
Max continuous pin current, any control or drive pin	±10mA

Voltage forced onto any pin -0.3V ~ (Vcc+ 0.3) Volts

* NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Electrical Characteristics

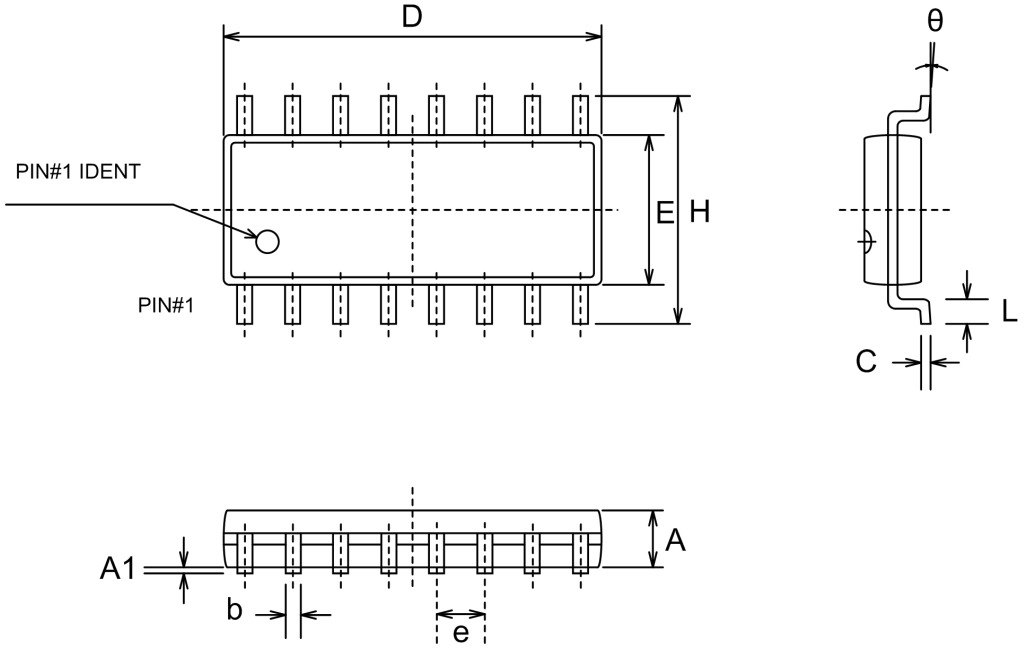
TA = 25℃

Characteristics	Symbo	Condition	Min	Typ	Max	Units
Operating voltage	Vcc		2.5		6.5	V
Current consumption	Idd	VCC=5.0V		1.15		mA
		VCC=3.0V		620		uA
		VCC=5.0V &SLEEP		40		uA
		VCC=3.0V &SLEEP		22		uA
Self calibration time after chip reset	Tini			300		ms
Range of capacitance on Pad	CX				2.5*CSEN	
Output impedance (open drain)	Zo	Low voltage		50		Ohm
		Hi-z		100M		
Output sink current	Isk	VCC=5V			10.0	mA
Minimum detective capacitance difference	delta_CX	CSEN=15pf		0.2		pF
Sample cycle	Tsi	Normal working state		13		ms
Time of Enter IDLE state	Tidle	No key		75		s

ESD Characteristics

Mode	Polarity	Max	Reference
H.B.M	POS/NEG	8000V	VDD
		8000V	VSS
		8000V	P to P
M.M	POS/NEG	500V	VDD
		500V	VSS
		500V	P to P

Package Diagram (SO-16)



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.30	1.50	1.70	0.051	0.059	0.067
A1	0.06	0.16	0.26	0.002	0.006	0.010
b	0.30	0.40	0.55	0.012	0.016	0.022
C	0.15	0.25	0.35	0.006	0.010	0.014
D	9.70	10.00	10.30	0.382	0.394	0.406
E	3.75	3.95	4.15	.0148	0.156	0.163
e	--	1.27	--	--	0.050	--
H	5.70	6.00	6.30	0.224	0.236	0.248
L	0.45	0.65	0.85	0.018	0.026	0.033
θ	0°	--	8°	0°	--	8°